(b) depositing one or more conductive materials to fill at least a portion of the feature definition;

(c) planarizing the one or more conductive materials to expose the dielectric material;

(d) removing at least a portion of the dielectric material; and

(e) depositing a low k dielectric material.

2. (Amended) The method of claim 1, wherein forming a feature definition in a dielectric material comprises:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) depositing a third dielectric layer on the second dielectric material;

(d) etching the first, second, and third dielectric layers to form a vertical interconnect; and

(e) etching the third dielectric layer to form a horizontal interconnect.

3. The method of claim 2, wherein the first and third dielectric layers comprises silicon oxide.

4. The method of claim 2, wherein the second dielectric layer is an etch stop.

5. The method of claim 4, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

6. The method of claim 1, wherein forming a feature definition in a dielectric material comprises:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) etching the second dielectric layer to exposed a portion of the first dielectric layer;

(d) depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer; and

(e) etching the first and third dielectric layers to form a vertical interconnect and to form a horizontal interconnect.

7. The method of claim 2, wherein the first and third dielectric layers comprises silicon oxide.

8. The method of claim 2, wherein the second dielectric layer is an etch stop.

9. The method of claim 4, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

10. The method of claim 1, further comprising depositing a low k barrier layer on the surface of the substrate prior to depositing the dielectric material.

11. The method of claim 10, wherein the low k barrier layer deposited on the surface of the substrate comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

12. The method of claim 1, wherein depositing the one or more conductive materials comprises depositing a conductive barrier layer of a first conductive material and then depositing a second conductive material on the conductive barrier layer.

13. The method of claim 12, wherein the first conductive material and the second conductive material are deposited by chemical vapor deposition, physical vapor deposition, or a electrochemical deposition technique.

14. The method of claim 12, wherein the first conductive material comprises one or more materials selected from the group of titanium, titanium nitride, titanium silicon

nitride, tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

15. The method of claim 12, wherein the second conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

16. The method of claim 1, wherein the low k dielectric material comprises a silicon and carbon containing material.

17. The method of claim 16, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

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18. The method of claim 1, further comprising depositing a low k barrier layer prior to depositing the low k dielectric material.

19. The method of claim 18, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

20. (Amended) The method of claim 1, wherein planarizing the one or more conductive materials comprises chemical mechanical polishing the one or more conductive materials.

21. The method of claim 1, further comprising planarizing the substrate surface after depositing the low k dielectric layer.

22. The method of claim 1, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

23. The method of claim 2, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

24. The method of claim 6, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

25. (Amended) A method for forming a dual damascene interconnect, comprising:

(a) depositing one or more dielectric layers on a substrate;

(b) etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect;

(c) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(d) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(e) planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers;

(f) removing at least a portion of the one or more dielectric layers;

(g) depositing a low k dielectric material; and

(h) depositing a self-planarizing dielectric layer on the low k dielectric material.

26. The method of claim 25, further comprising etching the low k dielectric material and the self-planarizing dielectric layer to form a dual damascene definition.

27. The method of claim 26, further comprising repeating steps (c) through (e).

28. The method of claim 25, wherein the one or more dielectric layers comprise silicon oxide, silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

29. The method of claim 25, wherein the conductive barrier layer comprises a material selected from the group of titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

30. The method of claim 25, wherein the conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

31. The method of claim 25, wherein the low k dielectric material comprises a silicon and carbon containing material.

32. The method of claim 31, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

33. The method of claim 25, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

34. The method of claim 25, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

35. The method of claim 25, further comprising depositing a low k barrier layer prior to depositing the dielectric material.

36. The method of claim 35, wherein the low k barrier layer deposited on the surface of the substrate comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

37. The method of claim 25, further comprising depositing a low k barrier layer prior to depositing a low k dielectric material.

38. The method of claim 37, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

39. The method of claim 25, wherein etching the one or more dielectric layers comprises etching the first and second dielectric layers to form a vertical interconnect and etching the third dielectric layer to form a horizontal interconnect.

40. The method of claim 25, further comprising performing a chemical mechanical polishing process on the substrate.

41. (Amended) A method for forming a dual damascene interconnect, comprising:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) etching the second dielectric layer to exposed a portion of the first dielectric layer;

(d) depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer;

(e) etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition;

(f) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(g) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(h) planarizing the conductive barrier layer and the conductive material to expose the one or more dielectric layers;

(i) removing the one or more dielectric layers;

(j) depositing a low k dielectric material on the substrate; and

(k) depositing a self-planarizing dielectric layer on the low k dielectric material.

42. The method of claim 41, further comprising etching the low k dielectric material and the self-planarizing dielectric layer to form a dual damascene definition.

43. The method of claim 41, further comprising repeating steps (f) through (h).

44. The method of claim 41, wherein the first and third dielectric layers comprises silicon oxide.

45. The method of claim 41, wherein the second dielectric layer is an etch stop.

46. The method of claim 41, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

47. The method of claim 41, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

48. The method of claim 41, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

49. The method of claim 41, wherein the conductive barrier layer comprises a material selected from the group of titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

50. The method of claim 41, wherein the conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

51. The method of claim 41, wherein the low k dielectric material comprises a silicon and carbon containing material.

52. The method of claim 41, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

53. The method of claim 41, further comprising depositing a low k barrier layer prior to depositing a low k dielectric material.

54. The method of claim 53, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

55. The method of claim 1, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.

56. The method of claim 1, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm, maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

57. The method of claim 25, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.

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58. The method of claim 25, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm, maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

59. The method of claim 41, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.